WHAT IS CLAIMED IS:

1. A driving method of a display device having a light emitting element and expressing a gradation with a length of lighting time,

said display device comprising:

a control circuit comprises first to fourth signals, first and second memories, and a reading device and a writing device,

wherein said first signal shows a state of said writing device,

said second signal shows a state of said reading device,

said third signal selects the roles of writing and reading to whether said first memory or said second memory, and switches the roles of said first signal and said second signal when said first signal and said second signal become a second state,

said fourth signal holds said third signal, and

said first and second memories are given the roles of writing and reading respectively,

wherein said first signal is inputted to said reading device and said second signal is inputted to said writing device,

said first signal and said second signal are in the first state when said writing device is in a write operation, therefore, said third signal is not inverted and said fourth signal overwrites the state of said third signal,

said first signal becomes the second state when said writing device is in wait state and said second signal also becomes the second state to invert said third signal, the roles of said first and second memories are switched and said second signal returns to the first state again,

said fourth signal compares with said third signal and when the state of said third signal changes, the state of said first signal is returned to the first state and said writing device starts writing thereby, and

the reading device and the writing device are synchronized by a series of operations above.

2. A display device having a light emitting element and expressing a gradation with a length of lighting time,

said display device comprising:

a control circuit which converts provided data for displaying with time gradation method,

wherein said control circuit comprises:

first and second memories to store said data;

a writing device to read said data and write said data to said first memory or said second memory;

a reading device to read said data from said first memory or said second memory to output said data;

a means to decide the roles for writing and reading to said first memory and said second memory in accordance with the states of said writing device and said reading device; and

first memory selector and second memory selector to select a writing and a reading to said first memory and said second memory,

wherein said writing device and said reading device are synchronized thereby.

3. A display device according to claim 2,

wherein said memory, said memory selector, said reading device and said writing device are formed over a display portion and a substrate altogether.

4. A display device according to claim 2,

wherein said memory is implemented on FPC.

5. A display device according to claim 2,

wherein said memory is implemented over a substrate.

6. An electronic device comprising the display device of claim 2.

7. A display device having a light emitting element and expressing a gradation with a length of lighting time,

said display device comprising:

a control circuit which converts provided data into the signals for displaying with time gradation method,

wherein said control circuit comprises:

first and second memories to store said data;

a writing device to read said data and write said data to said first memory or said second memory;

a reading device to read said data from said first memory or said second memory to output said data;

a means to decide the roles for writing and reading to said first memory and said second memory in accordance with the states of said writing device and said reading device; and

a memory selector for writing and a memory selector for output to select a writing and a reading to said first memory and said second memory,

wherein said means to decide the roles for writing and reading to said memories comprises:

a circuit which switches said first memory and said second memory selected by said memory selector for writing and said memory selector for output at the point said writing device finishes writing into said first memory or said second memory selected by said selector for writing, and said reading device finishes reading from said first memory or said second memory selected by said selector for output; and

a circuit which recognizes whether said first or second memories selected by said memory selector for output are switched at the point when said writing device finishes writing into said first or second memories selected by said selector for writing, besides said writing device finishes reading from said first or second memories selected by said memory selector for output, and makes said writing device into the state of writing when said first and second memories are switched by said memory selectors for writing and output,

wherein said writing device and said reading device are synchronized thereby.

8. A display device according to claim 7,

wherein said memory, said memory selector, said reading device and said writing device are formed over a display portion and a substrate altogether.

9. A display device according to claim 7,

wherein said memory is implemented on FPC.

10. A display device according to claim 7,

wherein said memory is implemented over a substrate.

11. An electronic device comprising the display device of claim 7.

12. A display device having a light emitting element and expressing a gradation with a length of lighting time,

said display device comprising:

first and second memories;

a conversion circuit to convert video signals from serial to parallel; and

first switch and second switch,

wherein the video signal is inputted to said first memory or said second memory through said first switch after converted to parallel by said conversion circuit, and

an output signal of said first memory or said second memory is inputted to a display through said second switch.

13. A display device according to claim 12,

wherein said memory is implemented on FPC.

14. A display device according to claim 12,

wherein said memory is implemented over a substrate.

15. An electronic device comprising the display device of claim 12.

16. A driving method of a display device comprising:

a control circuit comprising:

a first memory;

a second memory, wherein said first and second memories are given the roles of writing and reading respectively;

a writing device wherein a first signal includes an information about a state of said writing device; and

a reading device wherein a second signal includes an information about a state of said reading device,

wherein said first signal and said second signal are in the first state when said writing device is in a write operation, and

said first signal becomes a second state when said writing device is in a wait state and said second signal also becomes the second state so that the roles of said first and second memories are switched and said second signal returns to the first state again, and the state of said first signal is returned to the first state and said writing device starts writing.